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Sub E 1

C 1

1. (Amended) A transistor comprising:
a channel region;
a first gate on top of said channel region;
a second gate below said channel region; and
an isolation layer below said second gate,
wherein said first gate and said second gate are self-aligned and electrically separated from each other.

C 2

11. (Amended) A semiconductor chip having at least one transistor, said transistor comprising:
a channel region;
a first gate on top of said channel region;
a second gate below said channel region; and
an isolation layer below said second gate,
wherein said first gate is self-aligned with and comprises a different material than said second gate.

Please cancel claims 21-43.

Sub E 2 **Please add the following new claims:**

C 3

44. A transistor comprising:
a channel region;
a first gate on top of said channel region;
a second gate below said channel region;
an isolation layer below said second gate; and
source and drain regions laterally adjacent said channel region,

wherein said source and drain regions are self-aligned with said first gate and said second gate, such that said source and drain regions do not horizontally overlap said first gate or said second gate, and

wherein said first gate and said second gate are electrically separated from each other.

45. A transistor comprising:

a channel region;

a first gate on top of said channel region;

a second gate below said channel region;

an isolation layer below said second gate; and

source and drain regions laterally adjacent said channel region, said first gate, and said second gate,

wherein said first gate and said second gate are electrically separated from each other.

46. The transistor in claim 1, wherein said self-aligned nature of said first gate and said second gate positions said first gate above and aligned with said second gate.

47. The transistor in claim 4, further comprising:

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and

source and drain dielectrics between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

48. The semiconductor chip in claim 11, further comprising source and drain regions laterally adjacent said channel region, wherein said source and drain regions are self-aligned with said

first gate and said second gate, such that said source and drain regions do not horizontally overlap said first gate or said second gate.

49. The semiconductor chip in claim 11, wherein said self-aligned nature of said first gate and said second gate positions said first gate above and aligned with said second gate.

50. The semiconductor chip in claim 11, further comprising source and drain regions laterally adjacent said channel region, said first gate, and said second gate.

51. The semiconductor chip in claim 14, further comprising:

source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and

source and drain dielectrics between said source and drain regions and said first gate and said second gate,

wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.